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APPLICATION NUMBER: *60/477,542*
FILING DATE: *June 11, 2003*

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17231 U.S. PTO 06/11/03

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PTO/SB/16 (02-01)

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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53 (c).

Express Mail Label No. EV 335 816 676 Date of Deposit: JUNE 11, 2003

17613 U.S. PTO 60/477542

INVENTOR(S)

Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
THEODORE	LETAVIC	PUTNAM VALLEY, NY

☐ *Additional inventors are being named on the _____ separately numbered sheets attached hereto*

TITLE OF THE INVENTION (280 characters max)

"HIGH-SIDE CMOS IN AN INTEGRATED SOI PROCESS"

CORRESPONDENCE ADDRESS

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Address					
City	BRIARCLIFF MANOR	State	NY	ZIP	10510
Country	USA	Telephone	(914) 945-6000	Fax	(914) 332-0615

ENCLOSED APPLICATION PARTS *(check all that apply)*

☒ Specification *Number of Pages* 7 ☐ CD(s), Number

X Drawing(s) *Number of Sheets* 3 X Other (specify) IDS

☐ Application Data Sheet. See 37 CFR 1.76

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT *(check one)*

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check or money order is enclosed to cover the filing fees

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Respectfully submitted,

SIGNATURE [signature] Date 6/11/03

TYPED or PRINTED NAME STEVEN R. BIREN

REGISTRATION NO.: 26,531 *(if appropriate)*

TELEPHONE (914) 333-9630

Docket Number: US030162

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is used by the public to file (and by the PTO to process) a provisional application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the complete provisional application to the PTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C., 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Box Provisional Application, Assistant Commissioner for Patents, Alexandria, VA 22313.

HIGH-SIDE CMOS IN AN INTEGRATED SOI PROCESS

TECHNICAL FIELD

This invention relates to CMOS devices, and more specifically, to a technique of achieving elimination of the parasitic MOS channel present in thin film CMOS devices configured in the source, or what is called the source follower, configuration. Also disclosed is a methodology of performing a deep N implant in order to effectuate the inventive structure. Although most applicable in PMOS devices, the invention may also be utilized in the NMOS configuration.

BACKGROUND AND SUMMARY OF THE INVENTION

Figure 1 shows a thin film CMOS device including a source 101, drain 102, and MOS gate region 103. The SOI layer 104 forms an MOS junction 105 with an buried oxide layer 106. Below buried oxide layer 106 is a substrate layer 107, which would typically be several hundred microns thick. On the scale shown in Figure 1, the substrate layer 107 is too thick to depict and thus is not fully shown.

In source follower mode, sometimes called source high mode, the source 101 is biased with a voltage that is typically higher than the voltage at which substrate 107 is kept. This voltage difference could be over two hundred volts in typical applications. In thin film devices where the SOI layer 104 may be only slightly more than a micron thick, this voltage difference may be sufficient to induce an unwanted depletion region at or near the MOS junction 105. As shown therefore in Figure 1, a parasitic path 110 between source 101 and drain 102 exists at the MOS junction. This region creates a parasitic MOS channel, allowing leakage current to be conveyed between the source 101 and drain 101

when the real MOS gate region 103 is intended to be turned off. The device thus undesirably acts as if a second gate region existed, wherein the second gate is in the on state even when the actual gate region 103 is in the off state.

To date, there exists no known solution for stopping this leakage current when thin film SOI devices are utilized in the source follower configuration. Prior solutions all involve use of a much thicker SOI layer 104, rather than thin film devices. These prior devices have such a thick SOI layer that the depletion region resulting in the parasitic MOS channel 110 does not occur. However, in thin film applications the region 110 acts as a second current path in addition to the normal gate region.

There exists a need in the art for a technique of eliminating this parasitic channel 110 in source follower configurations with thin film SOI devices.

In complimentary arrangements, (i.e. using NMOS devices in which the source is biased much lower than the substrate) a similar problem may exist.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a depiction of a prior art CMOS thin film device, showing a parasitic MOS channel 110;

Figure 2 is a conceptual depiction of a device fabricated in accordance with the present invention; and

Figures 3A – D depict doping concentrations at various locations throughout the device.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 2 depicts an exemplary PMOS device including the deep N layer 201 placed below the source region 101. A substrate region 107 is maintained at an exemplary voltage of –200, over 200 volts lower that the typical voltage at which the source is biased. Due to the relatively thin SOI layer 104, (slightly more than 1 micron) a parasitic MOS channel 110 results from a depletion region that forms between the drain 102 and source 101 as indicated in Figure 1. However, the deep N layer 201 shown directly below the source region 101 prevents full depletion and instead forms the space charge neutral region 205 as indicated in dotted outline in Figure 2. This space charge neutral region205 prevents current flow between the source 101 and drain 102 along any parasitic channel than may otherwise be formed across MOS channel 110.

In the preferred embodiment, the implantation of the deep N layer 201 should be accomplished using a doubly ionized implant of 31P++ and a 200 KeV implant machine. This gives 400 KeV implant energy, without the need for a high energy implant machine.

It is also noted that while the deep N layer is shown below the source region 101 in Figure 2, it is noted that the space charge neutral region 205 may be implemented anywhere along what would otherwise be the parasitic current path 110 between the source 101 and drain 102. Thus, the deep N layer 201 may be placed directly below drain region 102, rather than below source region 101.

While the device has principal application in source high PMOS configurations, the complimentary device may be implemented in NMOS as well. Such an MMOS device would involve the P implant below the source or drain in similar concentration to those already

described, and would be applicable in arrangements where the bias configuration of the device is the reverse of what has been described herein with respect to PMOS devices.

Figures 3A – D show further manufacturing information regarding the implementation of the present invention in a PMOS device. Fig. 3A depicts a cross section showing the relative thickness' of the various portions of the device previously described. The device depicted in 3A is doped in concentrations profiled in Figure 3B. Note that Figures 3C and 3D compare the doping concentrations present in the source and drain regions respectfully. Note the concentration of the doping in the deep N region is shown is Figure 3D as being approximately 1 order of magnitude higher than the concentration shown in Figure 3B for the Nwell, the gate region.

It is noted that while the above describes the preferred embodiment of implementing the invention, various modifications and additions will be apparent for those that are skilled in the art. Such modifications are intended to be covered by the claims appended hereto.)

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WHAT IS CLAIMED IS:

1. A thin film Silicon on Insulator (SOI) device comprising a source, a gate, a drain, an SOI layer, and a substrate layer, the substrate layer being maintained at a potential enough lower than the source so that a parasitic MOS channel is formed between the source and drain; and a Deep N implant layer formed between either the source or drain and the parasitic MOS channel to prevent the flow of current between the source and drain via the parasitic MOS channel when the device is in an off state.

2. The device of claim 1 wherein the Deep N implant layer is formed between the source and the parasitic MOS channel.

3. The device of claim 1 wherein the Deep N implant layer is formed between the drain and the parasitic MOS channel.

4. A thin film Silicon on Insulator (SOI) device comprising a source, a gate, a drain, an SOI layer, and a substrate layer, the SOI layer being maintained at a potential enough higher than the source so that a parasitic MOS channel is formed between the source and drain; and a Deep P implant layer formed between either the source or drain and the parasitic MOS channel to prevent the flow of current between the source and drain via the parasitic MOS channel when the device is in an off state.

5. The device of claim 1 wherein the Deep P implant layer is formed between the source and the parasitic MOS channel.

6. The device of claim 1 wherein the Deep P implant layer is formed between the drain and the parasitic MOS channel.

7. A method of isolating the source and drain of an MOS device to avoid a parasitic MOS channel being formed comprising adding a double ionized 31P++ implant to form a deep N layer beneath the drain or source of the MOS device, thereby preventing current

flow across a parasitic MOS channel formed in said MOS device when the device is in an off state.

8. The method of claim 7 wherein said device includes a buried oxide layer, and wherein said parasitic MOS channel forms at or near the buried oxide layer – silicon layer interface.

9. The method of claim 7 wherein the doping concentration of the deep N layer is approximately one order of magnitude higher than that of the NWell layer on the device.

10. A CMOS device comprising source and drain regions adjacent to a buried oxide layer and separated by a gate region, the buried oxide layer being adjacent to a substrate layer, and an implant layer of particles directly below the drain or source such that when the difference in potential between the substrate and the source exceeds 200 volts, a parasitic MOS channel is induced across the gate region and the implant layer isolates said parasitic MOS channel from said drain region to thereby prevent current flow between said source and drain via said parasitic MOS channel.

11. The device of claim 10 wherein the ionized particles are implanted using approximately 200keV of energy.

ABSTRACT

An Silicon on Insulator device is disclosed wherein a parasitic channel induced in a thin film portion of the device is prevented from allowing current flow between the source and drain by a Deep N implant directly below the source of drain. The deep N implant prevents a depletion region from being formed, thereby cutting off current flow between the source and the drain that would otherwise occur.

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☒ Declaration Submitted With Initial Filing OR ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	PHUS030162WO
First Named Inventor	THEODORE LETAVIC
COMPLETE IF KNOWN	
Application Number	/
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

HIGH-SIDE CMOS IN AN INTEGRATED SOI PROCESS

the specification of which *(Title of the Invention)*

☒ is attached hereto

OR

☐ was filed on (MM/DD/YYYY) [ ] as United States Application Number or PCT International Application Number [ ] and was amended on (MM/DD/YYYY) [ ] (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY) Country	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

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NAME OF SOLE OR FIRST INVENTOR:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle [if any]) THEODORE	Family Name or Surname LETAVIC		
Inventor's Signature	Date		
PUTNAM VALLEY Residence: City	NY State	USA Country	USA Citizenship
25 BELL HOLLOW ROAD Mailing Address			
PUTNAM VALLEY City	NY State	10579 Zip	USA Country
NAME OF SECOND INVENTOR:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle [if any])	Family Name or Surname		
Inventor's Signature	Date		
Residence: City	State	Country	Citizenship
Mailing Address			
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☐ Additional inventors are being named on the _____ supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.

SD3-V3542-061103

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

THEODORE LETAVIC

Atty. Docket

US030162

Serial No.

Filed: CONCURRENTLY

Title: HIGH-SIDE CMOS IN AN INTEGRATED SOI PROCESS

Commissioner for Patents
Alexandria, VA 22313

APPOINTMENT OF ASSOCIATES

Sir:

The undersigned Attorney of Record hereby revokes all prior appointments (if any) of Associate Attorney(s) or Agent(s) in the above-captioned case and appoints:

STEVEN R. BIREN **(Registration No. 26,531)**

c/o U.S. PHILIPS CORPORATION, Intellectual Property Department, 580 White Plains Road, Tarrytown, New York 10591, his Associate Attorney(s)/Agent(s) with all the usual powers to prosecute the above-identified application and any division or continuation thereof, to make alterations and amendments therein, and to transact all business in the Patent and Trademark Office connected therewith.

ALL CORRESPONDENCE CONCERNING THIS APPLICATION AND THE LETTERS PATENT WHEN GRANTED SHOULD BE ADDRESSED TO THE UNDERSIGNED ATTORNEY OF RECORD.

Respectfully,

Michael E. Marion, Reg. 32,266
Attorney of Record

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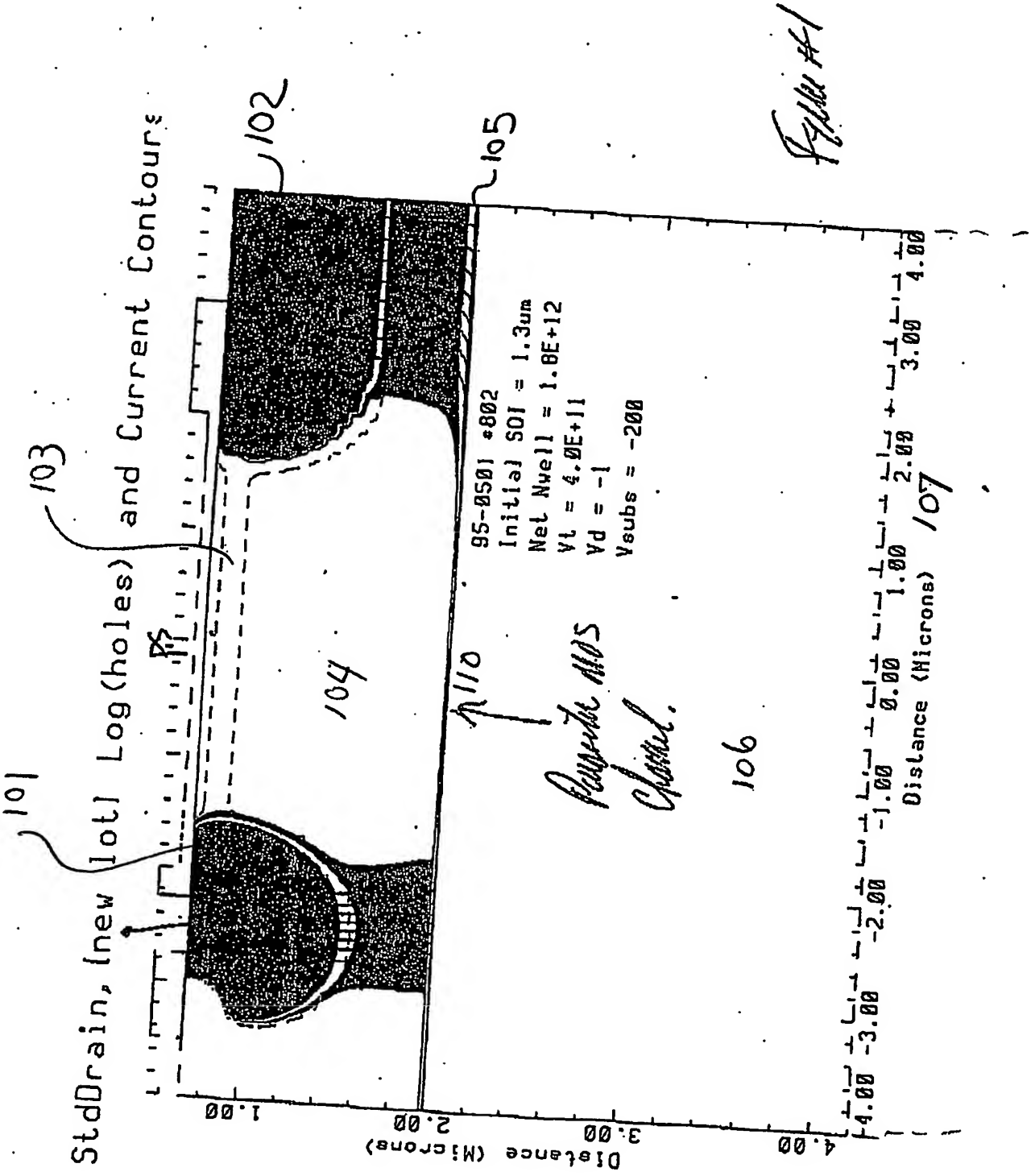
Figure #1
and Current Contours
Total Log(holes)
StdDrain, Inew
101
102
103
104
105
106
107
110
95-0501 #802
Initial SOI = 1.3um
Net Nwell = 1.8E+12
Vt = 4.0E+11
Vd = -1
Vsubs = -200
Distance (Microns)
1.00
2.00
3.00
4.00
-4.00
-3.00
-2.00
-1.00
0.00
1.00
2.00
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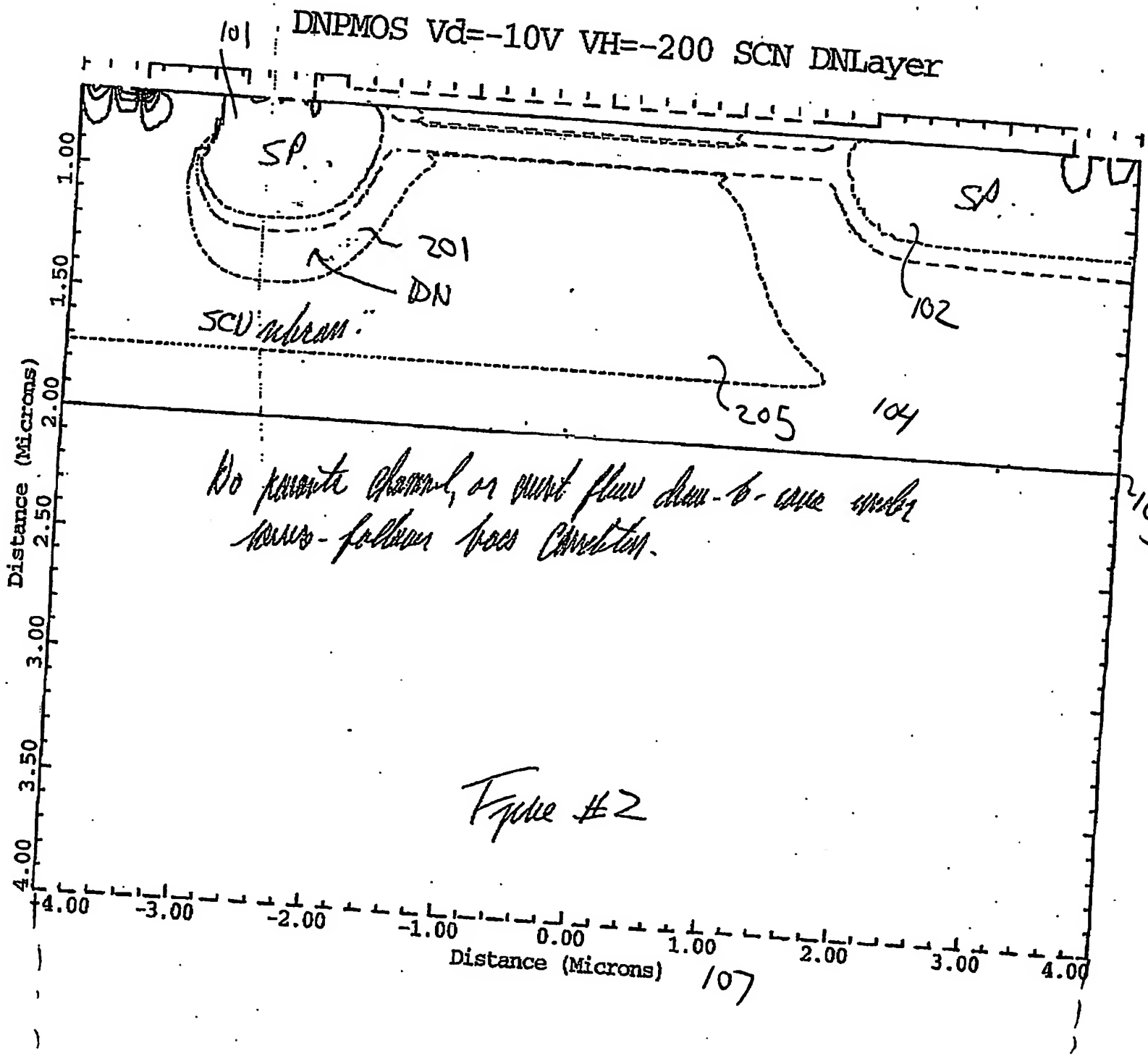

Do parasitic channel, or punch flow due-to-case under source-follower bias Condition.

Figure #2

PMOS 400keV 5e12 1e15SP Xgrid

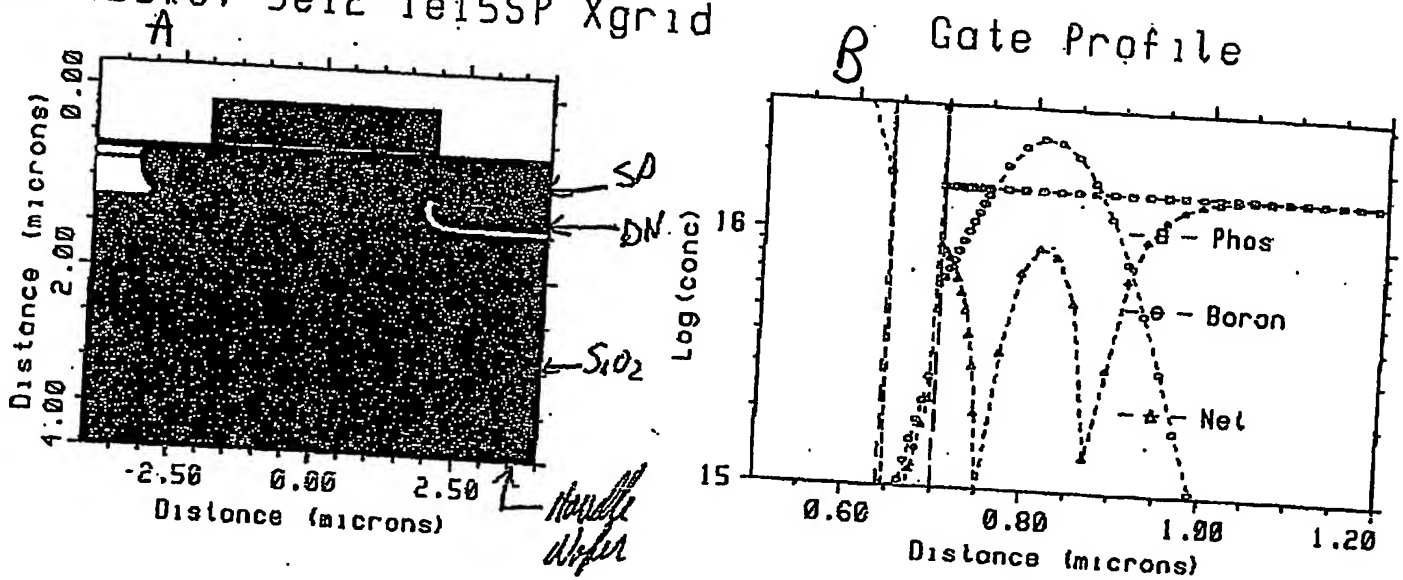

Figure #3

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